

CLAIMS

What is claimed is:

1. Apparatus comprising:
an array of computational cells coupled to one another and having a one-to-one correspondence with respective buffers of an array of buffers, wherein each computational cell includes:
a first input for receiving data corresponding to an availability status of the respective buffer corresponding to the computational cell;
a second input for receiving data corresponding to a currently selected buffer from among the array of buffers; and
a first output upon which data is produced for identifying a next available buffer,
wherein the data produced on the first outputs of the computational cells collectively comprise a next available buffer vector that identifies a next buffer in the buffer array to be allocated.
2. The apparatus of Claim 1, wherein each computational cell further comprises:
a third input; and
a second output coupled to the third input of a next computational cell,
wherein data is produced on the second output of a given computational cell as a function of data received at the first, second, and third inputs for the computational cell.
3. The apparatus of Claim 2, wherein each computational cell comprises:

2 an inverter for receiving data on the first input of the cell and having an
3 output;

4 a first AND gate having a first input coupled to the output of the inverter; and
5 a second input for receiving data on the third input of the cell, and having an output;

6 a second AND gate, having a first input for receiving data on the first input of
7 the cell and a second input for receiving data on the third input of the cell, said
8 second AND gate having an output corresponding to the first output of the cell; and

9 an OR gate, having a first input coupled to the output of the first and gate,
10 and a second input for receiving the data on the second input of the cell, said OR
11 gate having an output corresponding to the second output of the cell.

1 4. The apparatus of Claim 2, wherein the first input of a given computational cell
2 is labeled A, the second input is labeled P, the third input is labeled I, the first output
3 is labeled N, and the second output is labeled O, and further wherein each
4 computational cell produces a logic value at its first output N based on the logic
5 equation,

$$N = A \text{ AND } I$$

7 and wherein each cell produces a logic value at its second output O based on the
8 logic equation,

$$O = P \text{ OR } (\text{NOT } A \text{ AND } I).$$

1 5. The apparatus of Claim 2, wherein a plurality of computational cells are
2 arranged in a cascaded order so as to define 0th to Nth computational cells such that
3 the second output from an ⁱth computational cell is coupled to the third input of an (ⁱth
4 + 1) computational cell, and the second output from the Nth computational cell is
5 coupled to the third input of the 0th computational cell.

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1 6. The apparatus of Claim 1, wherein the array of buffers comprises N buffers
2 and data received at the first input of each computational cell collectively comprise
3 an availability vector comprising N bits, each bit corresponding to an availability
status of a respective buffer.

1 7. The apparatus of Claim 10, wherein the array of buffers comprises N buffers
2 and data received at the second input of each computational cell collectively
3 comprise a current selected entry vector comprising N bits, each bit corresponding
4 to a respective buffer, said current selected entry vector including only one bit that is
5 asserted, said asserted bit identifying a most recently allocated buffer.

1 8. The apparatus of Claim 1, wherein the array of buffers comprises N buffers
2 and the next available buffer vector comprises N bits, each bit corresponding to a
3 respective buffer, said next available buffer vector including only one bit that is
4 asserted, said asserted bit identifying the next available buffer to be allocated.

1 9. A processor comprising:
2 an array of buffers;
3 an array of computational cells coupled to one another in a cascaded fashion,
4 each computational cell corresponding to a respective buffer in the array of buffers
5 and including:
6 a first input for receiving data corresponding to an availability status of
7 a buffer corresponding to the computational cell;
8 a second input for receiving data corresponding to a currently selected
9 buffer from among the array of buffers;

10 a first output upon which data is produced for identifying a next
11 available buffer,
12 a second output; and
13 a third input, coupled to the second output of a preceding
14 computational cell,
15 wherein the data produced on the first outputs of the computational cells
16 collectively comprise a next available buffer vector that identifies the next buffer in
17 the buffer array to be allocated for use.

1 10. The processor of Claim 9, wherein said array of computational cells define 0th
2 to Nth computational cells, and the second output from the Nth computational cell is
3 coupled to the third input of the 0th computational cell.

1 11. The processor of Claim 2, wherein each computational cell comprises:
2 an inverter for receiving data on the first input of the cell and having an
3 output;
4 a first AND gate having a first input coupled to the output of the inverter; and
5 a second input for receiving data on the third input of the cell, and having an output;
6 a second AND gate, having a first input for receiving data on the first input of
7 the cell and a second input for receiving data on the third input of the cell, said
8 second AND gate having an output corresponding to the first output of the cell; and
9 an OR gate, having a first input coupled to the output of the first and gate,
10 and a second input for receiving the data on the second input of the cell, said OR
11 gate having an output corresponding to the second output of the cell.

1 12. The processor of Claim 9, wherein the first input of a given computational cell
2 is labeled A, the second input is labeled P, the third input is labeled I, the first output
3 is labeled N, and the second output is labeled O, and further wherein each
4 computational cell produces a logic value at its first output N based on the logic
5 equation,

$$N = A \text{ AND } I$$

7 and wherein each cell produces a logic value at its second output O based on the
8 logic equation,

$$O = P \text{ OR } (\text{NOT } A \text{ AND } I).$$

1 13. A method comprising:
2 determining an availability vector corresponding to an availability status of
3 buffers in an array of buffers;
4 determining a current selected entry vector that identifies a most recently
5 allocated buffer; and
6 determining a next available buffer vector that identifies the next available
7 buffer to be allocated from among the plurality of buffers as a function of the
8 availability vector and the current selected entry vector.

1 14. The method of Claim 13, wherein the array of buffers comprises N buffers
2 and the availability vector comprises N bits, each bit corresponding to an availability
3 status of a respective buffer.

1 15. The method of Claim 13, wherein the array of buffers comprises N buffers
2 and the current selected entry vector comprises N bits, each bit corresponding to a

